

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

- 5 Claim 1 (original): A semiconductor package which is positioned on a first substrate comprising:

- a second substrate having a first surface and a second surface;
- a chip positioned on the first surface of the second substrate;
- a plurality of first bonding balls positioned on the second surface of
- 10 the second substrate and arranged in a line along a first direction for connecting the second substrate to the first substrate; and
- at least a dummy bonding bar positioned on the second surface of
- the second substrate for connecting the second substrate to
- 15 the first substrate and preventing the semiconductor package from inclining to one side.

- Claim 2 (original): The semiconductor package of claim 1 wherein the second surface has a rectangular shape, and the first direction is parallel
- 20 to a long side of the second surface.

- Claim 3 (original): The semiconductor package of claim 2 wherein the longest side of the dummy bonding bar is approximately perpendicular to the long side of the second surface for preventing the semiconductor
- 25 package from inclining.

Claim 4 (original): The semiconductor package of claim 3 wherein a length of a short side of the second surface is less than 1000  $\mu\text{m}$ .

- 30 Claim 5 (original): The semiconductor package of claim 1 wherein the dummy bonding bar has a planar third surface connected to the first

substrate for preventing the semiconductor package from inclining.

Claim 6 (original): The semiconductor package of claim 1 further comprising a plurality of first bonding pads, each of which being  
5 positioned between the second surface and each of the first bonding balls, and at least a dummy bonding pad positioned between the second surface and the dummy bonding bar.

Claim 7 (original): The semiconductor package of claim 6 further  
10 comprising a plurality of second bonding pads positioned on the second surface and a plurality of second bonding balls respectively positioned on the second bonding pads, the second bonding balls being interlaced with the first bonding balls.

15 Claim 8 (original): The semiconductor package of claim 7 wherein a height of the dummy bonding bar is the same as a height of each of the first bonding balls and the second bonding balls.

Claim 9 (original): The semiconductor package of claim 7 wherein the  
20 first bonding balls, the second bonding balls and the dummy bonding bar respectively comprise a tin (Sn) based metal containing lead (Pb), and a melting point of the tin based metal is between 180°C and 235°C.

Claim 10 (original): The semiconductor package of claim 9 wherein the  
25 first bonding pads, the second bonding pads and the dummy bonding pad respectively comprise a tin based metal, which contains no lead and has a melting point between 180°C and 235°C.

Claim 11 (original): The semiconductor package of claim 1 wherein the  
30 first substrate comprises a build-up printed circuit board, a co-fired ceramic substrate, a thin-film deposited substrate, or a glass substrate.

**Claim 12 (original): The semiconductor package of claim 1 wherein the chip is an image sensor chip.**

**Claim 13-25 (canceled).**

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